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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,993	11/14/2001	Shunpei Yamazaki	SEL 291	9060

7590 12/02/2003

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EXAMINER	
TRAN, MINH LOAN	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,993	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Minhloan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *20-36* is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 17* is/are allowed.

6)☒ Claim(s) *1-7,11,12,15,18 and 19* is/are rejected.

7)☒ Claim(s) *8-10,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *02242003*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 02/24/2003 has been considered.

2. Applicant's communication filed on 09/08/2003 has been carefully considered by the examiner. The arguments advanced therein are persuasive with respect to the rejections of record and those rejections are accordingly withdrawn. In view of a further consideration and search, however, a new rejection is set forth further below. This action is not made final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 11, 12, 15, 18, 19 are rejected under 35 U.S.C. 103(a) as being obvious over Suzawa et al. (6,515,336).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

With regard to claims 1, 11, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. disclose a semiconductor device comprising at least a pixel portion and a driver circuit portion, the semiconductor device comprising a plurality of TFTS and each of TFTS comprising:

a semiconductor layer 103a formed on an insulating surface;

an insulating film 109 formed on the semiconductor layer 103a ; and

a gate electrode 110, 111 formed on the insulating film 109;

wherein the pixel portion comprises at least one TFT and the driving circuit portion has at least an n-channel TFT 201a and a p-channel TFT 200a;

wherein a gate electrode 119f of the n-channel TFT of the driving circuit portion has a laminate structure with a first conductive layer 119e as a lower layer and a second conductive layer 119d as an upper layer, the first conductive layer 119e having

a first width and a second conductive layer 119d having a second width that is narrower than the first width, and

wherein a gate electrode 122f of the TFT of at least the pixel portion has a laminate structure comprising a first conductive layer 122d and a second conductive layer 122e, an upper surface of the first conductive layer 122d and a lower surface of the second conductive layer 122e having the same width.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged.

With regard to claim 2, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the edge of the first conductive layer 119e of the n-channel TFT of the driving circuit portion is tapered in section.

With regard to claim 3, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the p-channel TFT of the pixel portion comprises a plurality of channel forming regions 222a, 222b, 228.

With regard to claim 4, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the n-channel TFT 201a of the driving circuit portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a channel forming region overlapping the gate electrode and an impurity region partially overlapping the gate electrode.

With regard to claim 5, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the impurity region of the n-channel TFT 201a has a region that has an impurity concentration gradient in a range of at least 1 x 10^{16} to 1x 10^{19} atoms/cm^3, and the impurity concentration thereof increases as the distance from the channel forming region 210 increases.

With regard to claim 6, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the impurity region of the n-channel TFT 201a includes a source region 213 or a drain region 212.

With regard to claim 7, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. show the TFT 204 of the pixel region has an LDD region 223a between the channel forming region 222a and a source region 225, or between the channel forming region 222a and a drain region 226.

With regard to claims 12, 15, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B,19A-19E of Suzawa et al. disclose a semiconductor device comprising at least a pixel portion and a driver circuit portion, the semiconductor device comprising a plurality of TFTS and each of TFTS comprising:

a semiconductor layer 103a formed on an insulating surface;

an insulating film 109 formed on the semiconductor layer 103a, and

a gate electrode 110, 111 formed on the insulating film 109;

wherein the pixel portion comprises at least one TFT 204 and the driving circuit portion has at least an n-channel TFT 201a and a p-channel TFT 200a;

wherein in the TFT 204 of the pixel portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a plurality of channel forming regions 222a overlapping the gate electrode 122f and an impurity region 223a partially overlapping the gate electrode 122f, and wherein in the n-channel TFT 201a of the driving circuit portion, the gate electrode has a tapered portion, and the semiconductor layer comprises a channel fonning region 210 overlapping the gate electrode and an impurity region 211 partially overlapping the gate electrode.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged.

With regard to claims 18 and 19, figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. further disclose the pixel portion comprises an electrode 148a, 148b formed on the second insulating film 143 and connected to the impurity region 225 of the TFT of the pixel portion; and a pixel electrode153a, 153b formed on the second insulating film 143 and comprising the same material as the electrode 148a, 148b.

Figures 1A-1D, 2A-2D, 3A-3C, 4A, 4B, 19A-19E of Suzawa et al. do not disclose the TFT of the pixel portion is a P-channel TFT. However, it would have been obvious to one of ordinary skill in the art to replace the NTFT by the PTFT because the NTFT and PTFT can be interchanged.

Allowable Subject Matter

4. Claims 8-10, 13, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 16, 17 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the gate wiring line comprises the same material as a pixel electrode connected to the impurity region of the p-channel TFT of the pixel portion.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minhloan T. Tran whose telephone number is (703) 308-4919. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mlt
11/2003

Minhloan T. Tran
Primary Examiner